REMARKS

Claims 1, 3-7, 9-12 and 14-23 are pending in the application of which Claims 16-20 were withdrawn from consideration. The Examiner rejects the Claims 1, 3-7, 9-12, 14, 15 and 21-23. The Examiner objects to the amendments to the Specification. Claims 7 and 21-23 are presently amended. Support for the amended claims can be found on pages 2, 4 and 6 of the application. No new matter has been introduced.

35 U.S.C. § 132 - NEW MATTER

The Examiner objects to the amendment filed on November 13, 2001, under 35 U.S.C. § 132 stating that a prior amendment introduced new matter. The Examiner states:

> 1. ... The added material which is not supported by the original disclosure is as follows: the phrase [1] "depositing an insulator layer of high temperature oxide ***directly*** on *the substrate and the floating gate*" and [2] "the insulator layer forming *sidewalls around the floating gate*" and [3] "the insulator layer forming *sidewalls of high quality oxide around the floating gate*".
>
> Applicant is required to cancel the new matter in the reply to this Office action.

Applicants respectfully traverse the Examiner's objection. The Examiner appears to object to the language of Claim 1 and Claim 23 as amended on November 13, 2001.

Objection [1]: "depositing an insulator layer of high temperature oxide ***directly*** on *the substrate and the floating gate*"

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First, the Examiner objects to the phrase "depositing an insulator layer of high temperature oxide ***directly*** on *the substrate and the floating gate*," which is contained in amended Claim 1. Claim 1 as originally filed recites, in part:

depositing an insulator on the substrate, the insulator covering the floating gate, a portion of the insulator not covering the floating gate having a second thickness that is greater than the first thickness;

During prosecution Claim 1 was amended to recite, in part:

depositing an insulator layer of high temperature oxide ***directly*** *on the substrate and the floating gate*, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming *sidewalls around the floating gate* to prevent charge leaking from the floating gate

For support of "depositing an insulator layer ... ***directly*** *on the substrate and the floating gate*," the Examiner's attention is directed to the originally filed Claims and Specification.

Original Claim 1 recites "depositing an insulator on the substrate" and "the insulator covering the floating gate, " which clearly support the amended claim language of "depositing an insulator layer ... ***directly*** *on the substrate and the floating gate.*"

not true

Further, the Specification discloses an embodiment of "a method of making a flash memory cell including a substrate having a floating gate ... includes depositing an insulator on the substrate. The insulator covers the floating gate." (Summary, page 2, lines 13-16.) For another embodiment, the Specification discloses "a flash memory cell includes a substrate having a tunnel oxide and a floating gate disposed on the tunnel oxide." (Summary, page 2, lines 27-29.) The Specification as filed supports the claim language "depositing an insulator layer ... ***directly*** *on the substrate and the floating gate.*"

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Objection [2]: "the insulator layer forming *sidewalls around the floating gate*"

Second, the Examiner objects to the phrase "the insulator layer forming *sidewalls around the floating gate*." Again, the Examiner's attention is directed to the originally filed Specification. Though the Specification does not use the precise phrase "forming sidewalls," it clearly describes the forming of sidewalls. Specifically, "Memory cell 10 further includes an insulator 30 on both sides of floating gate 16." (Detailed Description, page 3, lines 26-27.) Then ... "The oxidation process results in the formation of a layer of oxide (not shown) along the vertical side surfaces 17 of floating gate 16. The oxide seals side surfaces 17 of floating gate 16 to prevent any charge from escaping." (Detailed Description, page 4, lines 15-18.) Then again ... "Insulator 30 covers floating gate 16." (Detailed Description, page 4, lines 19-20.) The Specification as filed supports the claim language "the insulator layer forming *sidewalls around the floating gate*."

Objection [3]: "the insulator layer forming *sidewalls of high quality oxide around the floating gate*"

Third, the Examiner objects to the phrase "the insulator layer forming *sidewalls of high quality oxide around the floating gate*." The objected to quoted language is found in Claim 23. During prosecution independent Claim 23 was added and is presently amended. Amended Claim 23 recites, in part:

> depositing an insulator layer of high quality oxide on the tunnel oxide and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming *sidewalls of high quality oxide around the floating gate* to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by LPCVD process;

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As discussed above, the Specification supports "the insulator layer forming *sidewalls around the floating gate*" claim language. (Objection [2], above.) The Specification also supports "sidewalls of high quality oxide." Specifically, the Specification states: "Insulator 30 is preferably a high quality oxide which will prevent charge from leaking out vertical side surfaces 17 of floating gate 16." (Detailed Description, page 4, lines 25-26.) The Specification as originally filed supports the language objected to by the Examiner.

Reconsideration and allowance of the pending claims as amended are requested.

35 U.S.C. § 112 - FIRST PARAGRAPH

The Examiner rejected Claims 1, 3-7, 9-12, 14-15 and 21-23 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification. The Examiner states:

> [3.] Claims 1, 3-7, 9-12, 14-15, 21-23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. See new matter rejection above.

As discussed above, the Specification supports the amendments made to Claims 1 and 23. Reconsideration and allowance of the pending claims are thus requested. If the Examiner intents to maintain the rejections to Claims 1, 3-7, 9-12, 14-15, 21-23, the Examiner is requested to specifically point out what the Examiner considers "new matter" in the amended claims.

35 U.S.C. § 112 - SECOND PARAGRAPH

The Examiner rejected Claims 21 and 22 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states:

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[5.] Re claim 21, the term "the layer" lack[s] antecedent basis.
Re claim 22, the term "the layer" lack[s] antecedent basis.

The Applicant has amended the language of Claims 21 and 22 to more clearly reference "the layer of high temperature oxide" as "the insulator layer of high temperature oxide." Reconsideration and allowance of the pending claims are requested.

35 U.S.C. § 102(b) - ANTICIPATION: MITCHELL

The Examiner rejected Claims 1, 5, 7 and 11 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,713,142 ("Mitchell"). The Examiner states:

> [7.] Mitchell et al. discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layers, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layers, see figs. 1-5, cols. 1-6.

Applicants respectfully traverse the Examiner's rejections.

As per Claims 1 and 5, Mitchell does not teach "depositing an insulator layer of high temperature oxide ***directly*** on the substrate and the floating gate . . . to prevent charge leaking from the floating gate" as required by Claim 1 (emphasis added). To the contrary, Mitchell's insulator layer 37 is formed over an oxide layer 36, wherein oxide layer 36 is the layer that enhances "charge retention of the floating gate" (Mitchell, col. 2, line 68 and col. 3, lines 1-3). Claim 1 is thus distinguishable over the cited reference because Claim 1's single "insulator layer of high temperature oxide" accomplishes the same effect as the two separate layers 36 and 37 taught by Mitchell.

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Further, Claim 1 is further distinguished over Mitchell by reciting other limitations not disclosed or suggested by Mitchell. For example, according to Mitchell, neither the oxide layer 36 nor the insulator layer 37 is deposited to "a thickness greater than a thickness of the floating gate," as recited in Claim 1. As illustrated in Mitchell's figs. 2c and 2d of, oxide layer 36 is a very thin layer formed over the floating gate and the thickness of insulator layer 37, at best, is substantially the same as the thickness of the floating gate.

Additionally, the Examiner is relying on Mitchell's figures 2a, 2c and 2d in stating that the gate oxide layer is greater in thickness than the floating gate layer. When a reference does not disclose that the drawings are drawn to scale, arguments based on measurements of the drawing figures are of little value. See MPEP 2125. "[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue."[1] Here, Mitchell does not disclose that the figures are to scale and is completely silent as to the particular sizes of the layers. In fact, silicon dioxide layers 37 of Mitchell appears to be no higher than the top of polysilicon layer 33. Mitchell clearly does not contain enabling disclosure that would convey to one skilled in the art the limitations of Claim 1, and therefore, does not anticipate Claim 1.

As another example, Mitchell teaches two separate steps to form an oxide layer 36 and an insulator layer 37 over a floating gate. Mitchell's figure 2b shows "thermal oxidation to form silicon dioxide layer 36." Mitchell's silicon dioxide layer 36 deposited on the substrate is not of a thickness that is greater than the first thickness as required by Claim 1. Mitchell then discloses an intervening step of "ion implantation." (Mitchell, col. 3, lines 3-8.) Next, Mitchell discloses forming a "thick silicon dioxide layer 37. (Mitchell, col. 3, lines 8-12.) Silicon dioxide layer 37 acts to insulate, whereas silicon dioxide layer 36 acts to enhance a "charge retention of the floating gate" (Mitchell, col. 3, lines 1-3). But, the method in

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[1] *Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000).

accordance with Claim 1, advantageously, involves only one step to form a high temperature oxide serving to both insulate and prevent charges from leaking.

During the telephonic interview of October 3, 2001, the Examiner indicated that Claim 1 of Mitchell (column 4, lines 53-55) teaches "depositing a conformal layer of insulating material on the surface of said substrate and said conductive strips." Applicants submit that the Examiner is taking that teaching out of context. Taken as a whole, the cited reference teaches away from the present invention. For example, at column 4, lines 60-62, Mitchell discloses "forming a layer of ***conductive material*** on the surface of said conformal layer" (emphasis added). In contrast, Claim 1 of the present invention recites "depositing a ***dielectric*** layer on the planar surface" (emphasis added). Since a dielectric layer is NOT conductive, the cited reference, when read in its entirety, teaches away and is patentably distinguishable from Claim 1 of the present invention. Thus, for the above reasons, Applicants request reconsideration and allowance of Claims 1 and 5.

As per Claims 7 and 11, Applicants respectfully submit that Mitchell does not teach or suggest that "depositing an insulator layer of high temperature oxide directly on the tunnel oxide and the floating gate such that the insulator layer has a thickness that is greater than the first thickness," as recited in presently amended Claim 7. For substantially the reasons given above with respect to Claim 1, Claim 7 as amended and dependent Claim 11 are each allowable over the cited prior art. Thus, for the above reasons, Applicants request reconsideration and allowance of Claims 7 and 11.

35 U.S.C. § 102(e) - ANTICIPATION: Wu

The Examiner rejected Claims 1, 5, 7 and 11 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,033,956 ("Wu"). The Examiner states:

> [8.] Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator

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layer of oxide 210 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (inherently shows the insulator layer forming sidewalls around the floating gate to prevent charge leaking horn the floating gate, see fig. 2C), wherein the insulator layer is directly on the floating gate; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

Wu discloses the claimed invention except LPCVD oxide; the subject matter as a whole having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

Applicants respectfully traverse the Examiner's rejections.

As per Claim 1, Claim 1 recites, in part, "depositing an insulator layer of high temperature oxide." Similarly, Claim 7 recites, in part, "depositing an insulator layer of high temperature oxide." Wu, on the other hand, discloses a "conformal CVD TEOS (tetraethyl orthosilicate) oxide 210" rather than a high temperature oxide. Wu fails to disclose the invention.

Additionally, the Examiner recognizes that Wu fails to disclose all of the elements of the present invention. The Examiner states that "Wu discloses the claimed invention **except** LPCVD oxide." (Emphasis added.) Wu fails to disclose the invention, therefore, the § 102(e) rejection based on Wu is inappropriate. The Examiner is respectfully requested to withdraw the § 102(e) based on Wu. Reconsideration and allowance of the pending claims are thus requested.

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35 U.S.C. § 103(a) - OBVIOUSNESS

The Examiner rejected Claims 3, 4, 6, 9, 10, 12, 14, 15, 21, 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,033,956 ("Wu") or U.S. Patent 4,713,142

("Mitchell") taken with U.S. Patent 4,613,956 ("Paterson") in view of U.S Patent 5,808,339 ("Yamagishi") and the "applicant's admitted prior art." As per Claim 3, 4, 6, 9, 10, 12, 14, 15, 21, 22 and 23, the Examiner states:

> [11.] Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.
>
> Mitchell et al. discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-5, cols. 1-6.
>
> Wu and Mitchell et al disclosed the claimed invention except LPCVD oxide. Paterson et al. discloses a method for forming a semiconductor device, which includes depositing the high temperature/quality oxide on the floating gate by LPCVD in order to provide high uniformity and a highly doped floating gate (col. 3, lines 65-col. 4, lines 6 and col. 4, line 67-col. 5, line 47), see figs. 1-8c, cols. 1-10.
>
> The further difference between the instant claims and the prior arts is: polishing the insulator layer by CMP.
>
> Yamagishi et al. (figs. 9A-10D) discloses a method for forming a semiconductor device having a substrate 11 and a tunnel oxide 51 formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating

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gate 53; depositing an insulator layer of oxide 54 (by CVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing (using CMP or etching back; Art recognized equivalents: using CMP or etching back, because these two methods are art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one for another) the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 1 0A); and depositing a dielectric layer 55 (ONO) on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

The thickness of claims 3 and 9 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width; the rate of etching, temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in energy, etching rate, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality .... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller 105 USPQ233, 255 (CCPA 1955). *See also In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmscher* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any thickness range suitable to the method in process of Wu or Mitchell et al. in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Wu or Mitchell et al. with the teaching of Paterson et al. and Yamagishi et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device. In addition, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use

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LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

Claims 3, 4, 6, 21 and 22 are dependent on independent Claim 1. Claims 9, 10, 12, 14, 15 are dependent on independent Claim 7. As shown above, independent Claims 1 and 7 are allowable. Being dependent on allowable claims, dependent Claims 3, 4, 6, 9, 10, 12, 14, 15, 21 and 22 are also allowable.

Claim 23 recites, in part:

> depositing an insulator layer of high quality oxide on the tunnel oxide and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls of high quality oxide around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by LPCVD process

For the reasons explained above for the allowance of independent Claims 1 and 7, independent Claim 23 is also allowable. (See *supra*, ANTICIPATION: MITCHELL.) Reconsideration and allowance of the pending claims are thus requested.

35 U.S.C. § 103(a) - OBVIOUSNESS

The Examiner rejected Claims 1, 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15, 21, 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over U.S Patent 5,808,339 ("Yamagishi") or U.S. Patent 6,051,467 ("Chan") taken with Sze et al., "ULSI Technology" ("Sze") in view of "Applicant's admitted prior art." As per Claims 1, 3, 4, 6, 9, 10, 12, 14, 15, 21, 22 and 23, the Examiner states:

> [12.] Yamagishi et al. (figs. 9A-lOD) discloses a method for forming a semiconductor device having a substrate 11 and a tunnel oxide 51 formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 53; depositing an insulator layer of oxide 54 (by CVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater

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than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 1 0A); and depositing a dielectric layer 55 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-12B, cols. 1-16.

Chan et al. further discloses a method for forming a semiconductor device having a substrate 10 and a tunnel oxide 16 formed on the substrate, which comprises depositing a floating gate layer 18 on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 18; depositing an insulator layer of oxide 30 (by CVD methods, Le, APCVD or PECVD) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 5); and depositing a dielectric layer on the planar surface directly (layer 32 is a optional layer, which is well known in the art) over the exposed top surface of the floating gate and the insulator layer, see figs. 1-11, cols. 1-8.

However, the above references do not explicitly shows forming high temperature oxide by using LPCVD method (Note: during the telephone interview dated on 8/3/2001, applicant admitted that this layer is well known in the art and it is formed by LPCVD process, also see the amendment dated on 8/6/2001, furthermore, applicant stated in the specification, other dielectric may used, i.e., see page 3, lines 26-30. In addition, the disclosure fails to mention the criticality of the LPCVD process).

It is well known in the art to form the dielectric by using any CVD process. For example, Sze et al. teaches forming the dielectric by using LPCVD process, such will provide excellent purity and uniformity, confomal step coverage, large wafer capacity, high throughput, etc. Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

Furthermore, the thickness of claims 3 and 9 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as energy, dosage, thickness, width; the rate of etching, temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in energy, etching rate, thickness, dosage, temperature, or combination of any of them would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality .... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by

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routine experimentation." In re Aller 105 USPQ233, 255 (CCPA 1955). *See also In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmscker* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any thickness range suitable to the method in process of Yamagishi et al. or Chan et al. taken with Sze et al. and in view of Applicant's admitted prior art in order to optimize the process.

Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Yamagishi et al. or Chan et al. with the teaching of Sze et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device (also see above); in addition, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

Applicants respectfully traverse the Examiner's rejection. MPEP § 2143 provides:

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.[2] In particular, because none of the cited references suggests or discloses a "high temperature oxide" or an LPCVD process for forming a single oxide layer over a floating gate that can act to both insulate the floating gate and prevent charges from leaking, the Examiner

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[2] <u>In re Mills</u>, 916 F.2d 680 (Fed. Cir. 1990).

combination of Sze and the cited references can only be made by hindsight. Obviousness may not be established by hindsight reconstruction or conjecture.[3]

If the Examiner disagrees, Applicants respectfully request that the Examiner point out the suggestion or motivation to combine the cited references with more specificity in support of this § 103 rejection, as required under MPEP § 2143.01 and § 2143.03. A prima facie case of obviousness not being established, it is respectfully requested that § 103 rejection to be withdrawn.

Reconsideration and allowance of the pending claims are thus requested.

EXAMINER'S RESPONSE TO ARGUMENTS

The Examiner states:

13. Applicant's arguments filed 11/13/2001 have been fully considered but they are not persuasive.

Applicant argues that Mitchell et al. does not show depositing an insulator layer **directly** on *the substrate and the floating gate*. However, this is a new matter issue.

Applicant further argues that Mitchell et al. do not show forming the insulator layer having a thickness greater than the thickness of the floating gate. The Examiner disagrees because fig. 2C, layer 37 clearly shows this feature.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation

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[3] ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984).

to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Sze et al. teaches forming the dielectric by using LPCVD process, such will *provide excellent purity and uniformity, conformal step coverage, large wafer capacity, high throughput*, etc. Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

After considering this response, the Examiner is respectfully requested to find this application in condition for allowance. If there are any questions regarding this application, please call the undersigned at (408) 453-9200.

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Respectfully submitted,

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Version with markings to show changes made.

The following provides a marked up version of the amended claims containing the newly introduced changes. Additions are underlined and deletions are [bracketed]. Claims 7 and 21-23 are presently amended.

7. **(Four times amended)** A method of making a flash memory cell having a substrate and a tunnel oxide formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide directly on the tunnel oxide [substrate] and the floating gate such that the insulator layer has a thickness that is greater than the first thickness;

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

21. **(Amended)** The method of claim 1 wherein the insulator layer of high temperature oxide is formed by LPCVD process.

22. **(Amended)** The method of claim 7 wherein the insulator layer of high temperature oxide is formed by LPCVD process.

23. **(Amended)** A method of making a flash memory cell including a substrate, a tunnel oxide formed on the substrate and a floating gate, the method comprising:

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depositing an insulator layer of high quality oxide on the tunnel oxide [substrate] and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls of high quality oxide around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

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